IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant: **Bera, et al.** Case: **8477/ETCH/DRIE**

Serial No.: **10/663,304** Filed: **September 16, 2003**

Examiner: **Pham, Thanh V.** Group Art Unit: **2823**

Confirmation No.: **1356**

Title: **METHOD OF FABRICATING A DUAL DAMASCENE INTERCONNECT STRUCTURE**

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

CORRECTED APPEAL BRIEF

Pursuant to the Notification of Non-Compliant Appeal Brief dated on January 8, 2007, the Appellants submit this Corrected Appeal Brief to the Board of Patent Appeals and Interferences. This Corrected Appeal Brief is identical to the Appeal Brief filed on December 4, 2006 with the exception that the "Summary of Claimed Subject Matter" now includes citations to the Application as filed, as indicated as missing in the above-referenced Notification.

The Appellants believe that no fees are due in connection with this submission. However, the Commissioner is hereby authorized to charge counsel's Deposit Account No. 50-3562 for any fees, including extension of time fees, required to make this response timely and acceptable to the Office.

REAL PARTY IN INTEREST

The real party in interest is Applied Materials, Inc., located in Santa Clara, California.

RELATED APPEALS AND INTERFERENCES

The Appellants know of no related appeal and/or interference that may directly affect or be directly effected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-17 and 40-45 are pending in the application. Claims 1-17 and 40-45 stand rejected in view of several references as discussed below. The rejection of claims 1-17 and 40-45 based on the cited references is appealed. The pending claims are shown in the attached Appendix.

STATUS OF AMENDMENTS

No amendments to the claims were submitted in this application subsequent to final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention provides a method for fabricating a dual damascene interconnect structure. In the embodiment of independent claim 1, a method of fabricating an interconnect structure comprises (a) providing a substrate 200 having a film stack 201 comprising sequentially formed on the substrate 200 a first barrier layer 202, a conductive layer 216 embedded in a first dielectric layer 204, a second barrier layer 206, a second dielectric layer 208, and a cap layer 210 (*Specification*, ¶ [0018]; Figs. 1, 2A); (b) etching a via hole 224 in the cap layer 210 and the second dielectric layer 208 (*Id.*, ¶ [0025]; Figs. 1, 2C); (c) filling a portion of a depth 226 of the via hole 224 with a masking material (*Id.*, ¶ [0028]; Figs. 1, 2E); (d) etching in-situ the cap layer 210 (*Id.*, ¶ [0033]-[0034]; Figs. 1, 2H), a trench 218 in the second dielectric layer 208 (*Id.*, ¶ [0035]-[0036]; Figs. 1, 2I), the masking material (*Id.*, ¶ [0037]-[0038]; Figs. 1, 2J),

and the second barrier layer 206 (*Id.*, ¶ [0039]-[0040]; Figs. 1, 2K), by providing a plasma source power 318 of at least about 1000 Watts and a bias power 322 of at least about 800 Watts while etching during at least a portion of step (d) (*Id.*, ¶ [0036]); and (e) metallizing the via hole 224 and the trench 218 (*Id.*, ¶ [0041]; Figs. 1, 2L).

In the embodiment of independent claim 40, a method of etching comprises (a) providing a substrate 200 having a dielectric layer 204 to be etched on a substrate support 316 in a process chamber 310, the process chamber 310 having a plasma source electrode 328 disposed above the substrate support 316 and a substrate bias electrode disposed below a support surface of the substrate support 316 (*Id.*, ¶ [0018]; Figs. 1, 2A, 3); (b) providing an etch gas mixture 350 (*Id.*, ¶ [0036]; Figs. 1, 2I, 3); and (c) supplying a source power of at least about 1000 Watts at a frequency of above about 100 MHz to the plasma source electrode 328 and a bias power of at least about 800 Watts to the substrate bias electrode while etching the dielectric layer 204 (*Id.*, ¶ [0036]; Figs. 1, 2I, 3).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-6, 8-10 and 40-45 stand rejected under 35 U.S.C. §103(a) as being obvious in light of United States Patent No. 6,797,633, issued September 28, 2004, to *Jiang, et al.* (hereinafter *Jiang*) in view of United States Patent Application Publication Serial No. 2004/0161930, published August 19, 2004 to *Ma, et al.* (hereinafter *Ma*), and/or United States Patent No. 6,797,633, issued July 30, 2002 to *Ikeda* (hereinafter *Ikeda*).

2. Claims 7, 11-17 and 44-45 stand rejected under 35 U.S.C. §103(a) as being obvious in light of *Jiang* in view of *Ma* and/or *Ikeda*, as applied to claims 1-6, 8-10, and 40-45 above, and further in view of Taiwan Patent 544,815 published August 1, 2003 to *Chun, et al.* (hereinafter *Chun*), and United States Patent 6,177,147 issued on January 23, 2001 to *Samukawa, et al.* (hereinafter *Samukawa*).

ARGUMENT

1. Claims 1-6, 8-10 and 40-45

As noted above, claims 1-6, 8-10 and 40-45 presently stand rejected as being obvious in light of *Jiang* in view of *Ma* and/or *Ikeda*. The Appellants disagree.

To reject a claim under 35 USC §103, the initial burden is on the Examiner to create a *prima facie* case of obviousness. To do this, three basic criteria must be met: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; second, there must be a reasonable expectation of success; and third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. In addition, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must be found in the prior art, and must not be based on the Applicant's disclosure. *MPEP* §2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Independent claims 1 and 40 recite limitations not taught or suggested by any combination of the cited references. *Jiang* describes a method for forming a dual damascene trench patterning method. However, *Jiang* fails to teach or suggest etching in-situ the cap layer, a trench in the second dielectric layer, the masking material, and the second barrier layer, by providing a plasma source power of at least about 1,000 Watts and a bias power of at least about 800 Watts while etching, as recited in claim 1, or supplying a source power of at least about 1000 Watts at a frequency of above about 100 MHz to the plasma source electrode and a bias power of at least about 800 Watts to the substrate bias electrode while etching the dielectric layer as recited in claim 40.

Ma discloses a method of *in-situ* discharge prior to a plasma etch in order to avoid arcing within the chamber during the plasma etch process. (*Ma*, paragraph [0001].) *Ma* further discloses applying an RF power in the range of 100 to 1000 Watts for a 200 mm wafer and from 100 to 2000 Watts for a 300 mm wafer. (*Ma*, paragraph [0028].) However, *Ma* is silent regarding the bias power applied. As such, *Ma* fails to teach or suggest a modification of *Jiang*, alone or in combination with any of the other cited references, that would yield a plasma source power of at least 1,000 Watts and a

bias power of at least about 800 Watts while etching during at least a portion of the etch step, as recited in claims 1 and 40, respectively.

In addition, the present rejection is supported by the Examiner's contention that it would have been obvious to modify the etch steps of *Jiang* using the power, pressure, and flow rates as taught by the discharge sequence of *Ma* in order to avoid arcing during the plasma etch processes. However, *Ma* discloses that the discharge sequence is performed prior to the plasma etch process. (*Ma*, paragraph [0014]). Specifically, *Ma* states that no etching of the photoresist layer or substrate occurs during the discharge sequence. (*Ma*, paragraph [0028]). As such, *Ma* fails to teach or suggest any combination that results in providing these conditions while etching, as recited in claims 1 and 40. Accordingly, any combination of *Ma* and *Jiang* would result in a method wherein a discharge step that does not etch the substrate would be performed prior to plasma etching in order to avoid arcing. Thus, there is no suggestion to modify the etch steps of *Jiang* with the process conditions of the discharge sequence taught by *Ma*, in a manner that would yield the limitations recited in claims 1 and 40.

In the Response to Amendment section of the non-final Office Action dated February 24, 2006, the Examiner contends that "although not taught as a preferred embodiment, *Ma* teaches this embodiment nonetheless…." The Appellants respectfully disagree. Contrary to the Examiner's contention, *Ma* does not make a broad disclosure relating to bias and power conditions and then limit such disclosure to a "preferred embodiment" wherein the substrate is not etched during the discharge sequence.

Specifically, and as noted in the Response filed May 23, 2006, the motivation provided by the Examiner to combine the teachings of *Ma* ("to avoid arcing during plasma etch processes"), will yield an in-situ discharge step (during which *Ma* specifically states that no etching occurs) performed prior to etching in order to avoid arcing during the plasma etch process subsequently performed. The Examiner relies on *Ma* to support that "the method is extendable to etching low K dielectric layers." However, this statement merely reflects the fact that the discharge sequence may be performed at various stages throughout fabrication. For example, the Summary of the Invention section of *Ma* states that the discharge sequence may be beneficial when "etch transferring a pattern into a low k dielectric layer that has a poor thermal

conductivity and tends to produce arcing in conventional etch processes." (*Ma*, ¶[0016].) The teaching to use the discharge sequence (during which *Ma* teaches that no etching occurs) prior to etching a low k dielectric layer does not supply any teaching, suggestion, or motivation to provide a plasma source power of at least about 1,000 Watts and a bias power of at least about 800 Watts while etching, as recited in claims 1 and 40. Accordingly, *Ma* fails to teach or suggest modifying the cited references in the manner asserted by the Examiner.

In summary, *Ma* teaches that to avoid arcing during a plasma etch process, a discharge sequence is performed prior to the etch process. *Ma* fails to teach or suggest the limitations asserted by the Examiner in order to eliminate or reduce the incidence of arcing while etching. Therefore, because no etching of the photoresist layer or substrate occurs during the discharge sequence, any combination of *Ma* with *Jiang* for the purpose of reducing arcing during etching results in a method wherein the discharge step, that does not etch the substrate, is performed prior to plasma etching. Thus, *Ma* does not provide the modification proposed by the Examiner.

Ikeda discloses a method of manufacturing a semiconductor device wherein multiple etch steps are provided for etching different layers formed on a substrate. One step of the etch process provides 1600W of electricity to an upper electrode and 1400W of electricity to a lower electrode. The Examiner asserts that it would have been obvious to modify *Jiang* with the power, pressure, and flow rates as taught by *Ikeda* to "reduce the F radicals which form a hardened surface layer." (*Final Office Action* dated August 8, 2005, p. 6, ll. 3-11; *Office Action* dated February 24, 2006, p. 5, ll. 8-16.) The Appellants disagree.

Ikeda provides no suggestion or motivation to modify the etch process as taught by *Jiang* (alone or modified by *Ma*) in a manner that yields the limitations recited in claims 1 and 40 because, contrary to the Examiner's assertion, *Ikeda* fails to teach or suggest that providing a plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts will reduce F radicals in the process chamber. To provide the benefit that the Examiner cites ("to reduce F radicals which form a hardened surface layer"), *Ikeda* teaches that, in a parallel plate plasma etcher, "the upper electrode 703 is made of Si, which has high reactivity for F radicals. That is, the

excessively generated F radicals are trapped by Si of the upper electrode so that F radicals are reduced." (*Ikeda*, col. 2, ll. 40-44.)

In addition, *Ikeda* teaches that sputtered Si from the upper electrode may deposit on the photoresist and form a hardened resist surface layer. *Ikeda* further teaches that the electricity to the upper electrode should be removed, *i.e.*, the upper electrode should be grounded, to cause a reduction in excess Si atoms which prevents the hardened surface layer from being formed on the photoresist. (*Id.*, col. 5, ll. 61-67.) Therefore, if one wished to prevent the hardened surface layer from being formed on the photoresist, the upper electrode should be grounded. Therefore, to obtain the benefit of the motivation provided by the Examiner, *Ikeda* further teaches to ground the upper electrode. Thus, *Ikeda* teaches away from the modification proposed by the Examiner.

As such, the motivation provided by the Examiner, in both the non-final and final Office Actions, to combine *Ikeda* and *Jiang* would result in a process that is modified by either or both of forming an upper electrode of silicon and/or connecting the upper electrode to ground. As such, the combination of *Ikeda* and *Jiang* (alone or modified by any of the cited references) fails to yield a plasma source power of at least about 1,000 W and a bias power of at least about 800 W while etching during at least a portion of the etch step, as recited in claims 1 and 40.

In the Advisory Action dated November 22, 2005, the Examiner asserts that "the pointed to teachings of *Ikeda* do not negate the argument that *Ikeda* teaches the use of the recited bias power during at least a portion of the etch process... *i.e.*, the upper electrode would not be grounded during the entire etching step." This general assertion is restated in the Office Action dated February 24, 2006. However, the Appellants respectfully point out that the Examiner's rebuttal inappropriately presumes the combination. In other words, the Examiner rebuts the argument that there is no motivation to combine the references in the manner suggested by stating that, if combined, the references would teach the limitations recited in the claims.

The initial burden lies on the Examiner to create a *prima facie* case of obviousness, which requires that some suggestion or motivation exists, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. In addition, the

teaching or suggestion to make the claimed combination must be found in the prior art, and must not be based on the Applicant's disclosure. *MPEP* §2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." *MPEP* § 2143.01 (III) (citing *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990))(emphasis in original).

The requirement for providing a suggestion or motivation to combine the teachings of references is "rigorously applied" by the courts. (*In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999)("Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references."); *see also*, *In re Kotzab*, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000)("particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed")).

Examiners can satisfy this burden "only by showing some objective teaching in the prior art that would lead an individual to combine the relevant teachings of the references." (*In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992); *see also*, *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143 (Fed. Cir. 1985) (There must be some reason for the combination other than the hindsight gleaned from the invention itself to selectively combine prior art references to render a subsequent invention obvious.))

In the present case, the Examiner has not pointed to any "objective teaching" in *Ikeda* (or elsewhere) that would "lead an individual to combine the relevant teachings of the references." Specifically, as discussed above, *Ikeda* fails to provide any teaching, suggestion, or motivation to modify the teachings of *Jiang* with the plasma source and bias powers, as recited in claims 1 and 40, to obtain the benefit cited by the Examiner. The Examiner appears to be inadvertently and inappropriately using hindsight analysis to pick and choose teachings from the references to support the obviousness rejection. However, it is well-settled that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention."

(*In re Fine*,837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988)) Accordingly, the Appellants submit that the teachings of *Ikeda* cannot be combined with the remaining references in the manner suggested by the Examiner because there is no motivation or suggestion to do so.

The Examiner asserts in paragraph 9 (and again in paragraph 11) of the Final Office Action that the Appellants have found "a different mechanism to reduce F radicals." However, the Appellants note that, after careful review of *Ikeda*, the Appellants can find no support whatsoever for the contention that the teachings of *Ikeda* that the Examiner proposes to combine with *Jiang* and *Ma* provide the benefit that the Examiner asserts. *Ikeda* simply fails to provide any suggestion or motivation to modify the etch process as taught by *Jiang* (alone or as modified by *Ma*) in a manner that yields the limitations recited in claims 1 and 40.

The Examiner further asserts in paragraph 9 of the Final Office Action the pointed to teaching of *Ikeda* "does not negate the provided step II (e.g.) in Ikeda's Fig. 4." However, the Appellants respectfully note that, as acknowledged by the Examiner, there must be "some teaching, suggestion, or motivation to [make the proposed modification] found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art." In addition, in the Advisory Action dated August 31, 2006, the Examiner states that "it would have been obvious to employ the entire process conditions of *Ikeda* to enable the disclosed silicon oxide ILD etching step of *Jiang* to be performed [...] because *Ikeda* discloses the conditions are useful in etching silicon oxide dielectric layers." (See pg. 2, para. 4) (emphasis added). However, as noted above, "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." *MPEP* § 2143.01 (III) (citing *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990))(emphasis in original). Thus, the combination *Jiang*, *Ma*, and *Ikeda* fails to yield the limitations recited in the claims as required to establish a *prima facie* case of obviousness.

In summary, it is respectfully submitted that *Ikeda* and *Ma* fail to teach or suggest a modification to the teachings of *Jiang* that would result in the limitations recited in the present claims. Therefore, a *prima facie* case of obviousness has not been established

because any permissible combination of the cited references fails to yield all of the limitations recited in each of independent claims 1 and 40, and all claims respectively depending therefrom.

Thus, independent claims 1 and 40, and claims 2-6, 8-10 and 41-45, respectively depending therefrom, are patentable over *Jiang* in view of *Ma* and/or *Ikeda*. Accordingly, the Appellants respectfully request that the rejection be withdrawn and the claims allowed.

2. Claims 7, 11-17 and 44-45

As noted above, claims 7, 11-17 and 44-45 stand rejected as being obvious in light of *Jiang* in view of *Ma* and/or *Ikeda*, as applied to claims 1-6, 8-10, and 40-45 above, and further in view of *Chun* and *Samukawa.* The Appellants disagree.

Independent claims 1 and 40, from which the rejected claims depend, recite limitations not taught or suggested by any combination of the cited art. The patentability of claims 1 and 40 over *Jiang* in view of *Ma* and/or *Ikeda* has been discussed above. *Chun* discloses a process for etching a nitride layer and an oxide layer using O_2, N_2, and CF_4 in a ratio of O_2:N_2:CF_4 equal to 4-50:0-10:1. *Chun* further discloses applying an RF power in the range of 100 to 1000 Watts but is silent regarding any bias power applied. (*Chun*, Abstract.) However, *Chun* fails to teach or suggest a plasma source power of at least about 1,000 W and a bias power of at least about 800 W during at least a portion of the etch step, as recited in claims 1 and 40.

Samukawa similarly fails to teach or suggest a plasma source power of at least about 1,000 W and a bias power of at least about 800 W during at least a portion of the etch step, as recited in claims 1 and 40. *Samukawa* discloses a process and apparatus for treating a substrate using an ultra-high frequency (UHF) plasma. *Samukawa* further generally discloses applying a UHF RF power in the range of 0 to 1000 Watts. However, *Samukawa* is silent regarding the bias power applied. (*Samukawa*, Figs 3, 6-8, and accompanying text.) As both *Samukawa* and *Chun* fail to teach or suggest the missing limitations recited in the claims, neither *Samukawa* nor *Chun* teach or suggest a modification of any combination of *Jiang*, *Ma*, and *Ikeda*, that would yield all of the limitations recited in the claims.

Therefore, a *prima facie* case of obviousness has not been established because any permissible combination of the cited references fails to yield all of the limitations recited in each of independent claims 1 and 40, and claims 7, 11-17, and 44-45, respectively depending therefrom.

Thus, independent claims 1 and 40, and claims 7, 11-17, and 44-45, respectively depending therefrom, are patentable over *Jiang* in view of *Ma* and/or *Ikeda*, and further in view of *Chun,* and *Samukawa*. Accordingly, the Appellants respectfully request that the rejection be withdrawn and the claims allowed.

CONCLUSION

For the reasons advanced above, Appellants respectfully urge that the rejections of claims 1 -17 and 40-45 as being unpatentable under 35 U.S.C. §103 are improper. Reversal of the rejections in this appeal is respectfully requested.

Respectfully submitted,

January 22, 2007

/ Alan Taboada /

Alan Taboada
Attorney Reg. No. 51,359
(732) 935-7100
Moser IP Law Group
1040 Broad Street, 2nd Floor
Shrewsbury, NJ 07702

CLAIMS APPENDIX

1. (Previously Presented) A method of fabricating an interconnect structure, comprising:

(a) providing a substrate having a film stack comprising sequentially formed on the substrate a first barrier layer, a conductive layer embedded in a first dielectric layer, a second barrier layer, a second dielectric layer, and a cap layer;

(b) etching a via hole in the cap layer and the second dielectric layer;

(c) filling a portion of a depth of the via hole with a masking material;

(d) etching in-situ the cap layer, a trench in the second dielectric layer, the masking material, and the second barrier layer, by providing a plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts while etching during at least a portion of step (d); and

(e) metallizing the via hole and the trench.

2. (Original) The method of claim 1 wherein the cap layer comprises SiO_xN_y, where x and y are integers.

3. (Previously Presented) The method of claim 1 wherein the first dielectric layer and the second dielectric layer comprise at least one of carbon doped silicon oxide, organic doped silicon glass, and fluorine doped silicon glass.

4. (Previously Presented) The method of claim 1 wherein the first barrier layer and the second barrier layer comprise at least one of SiO_2, SiC, and Si_3N_4.

5. (Original) The method of claim 1 wherein the conductive layer comprises at least one of Cu, Al, Ta, W, Ti, TaN, and TiN.

6. (Original) The method of claim 1 wherein the masking material is selected from a group consisting of an organic material and photoresist.

7. (Original) The method of claim 1 wherein the step (b) further comprises:

forming a first patterned etch mask on the cap layer to define the via hole;

etching the via hole providing CF_4 and N_2 at a flow ratio CF_4:N_2 in a range from 1:1 to 1:5; and

stripping the first patterned etch mask.

8. (Original) The method of claim 1 wherein the step (c) further comprises:

applying the masking material to the substrate to fill the via hole; and

etching back the masking material until the masking material is removed from the via hole to a pre-determined depth that is smaller than a depth of the trench.

9. (Previously Presented) The method of claim 8 wherein the step (d) further comprises:

providing O_2 at a flow rate from about 100 to 1000 sccm;

maintaining a chamber pressure at about 5 to 200 mT; and

applying a cathode bias power between 100 and 400 W.

10. (Original) The method of claim 1 wherein the step (d) further comprises:

forming on the cap layer a second patterned etch mask to define the trench; and

stripping the second patterned etch mask contemporaneously with etching the masking material.

11. (Original) The method of claim 1 wherein the step (d) further comprises:

using a very high frequency (VHF) high-density plasma and a selectively controlled cathode bias power.

12. (Original) The method of claim 11 wherein the VHF is about 160 MHz.

13. (Previously Presented) The method of claim 12 wherein the cathode bias power is applied in a range from 0 to about 3000 W at a frequency in a range from about 50 kHz to 13.6 MHz during at least a portion of step (d).

14. (Original) The method of claim 11 wherein the step of etching the cap layer further comprises:

providing CF_4 and N_2 at a flow ratio CF_4:N_2 in a range from 1:1 to 1:5;

applying a source power between about 0 and 2000 W; and

applying a cathode bias power between 400 and 1200 W.

15. (Original) The method of claim 11 wherein the step of etching the trench further comprises:

providing CF_4 and N_2 at a flow ratio CF_4:N_2 in a range from 1:1.2 to 17:1;

applying a source power between about 1000 and 2000 W; and

applying a cathode bias power between 800 and 1800 W.

16. (Original) The method of claim 11 wherein the step of etching the masking material further comprises:

providing O_2 at a flow rate from about 300 to 1000 sccm;

maintaining a chamber pressure at about 5 to 200 mT;

applying a source power between about 200 and 2000 W; and

applying a cathode bias power between 100 and 400 W.

17. (Previously Presented) The method of claim 11 wherein the step of etching the second barrier layer further comprises:

providing CF_4 and N_2 at a flow ratio CF_4: N_2 in a range from 1:5 to 10:1;

applying a source power between about 200 and 600 W; and

applying a cathode bias power between 200 and 400 W.

18-39. (Cancelled)

40. (Previously Presented) A method of etching, comprising:

(a) providing a substrate having a dielectric layer to be etched on a substrate support in a process chamber, the process chamber having a plasma source electrode disposed above the substrate support and a substrate bias electrode disposed below a

support surface of the substrate support;

(b) providing an etch gas mixture; and

(c) supplying a source power of at least about 1000 Watts at a frequency of above about 100 MHz to the plasma source electrode and a bias power of at least about 800 Watts to the substrate bias electrode while etching the dielectric layer.

41. (Previously Presented) The method of claim 40, wherein the dielectric layer comprises at least one of carbon doped silicon oxide, organic doped silicon glass, and fluorine doped silicon glass.

42. (Previously Presented) The method of claim 40, further comprising:

maintaining a chamber pressure greater than about 100 mT.

43. (Previously Presented) The method of claim 40, wherein the chamber pressure is about 250 mT.

44. (Previously Presented) The method of claim 40, wherein step (c) further comprises supplying the source power at about 1,000 watts.

45. (Previously Presented) The method of claim 40, wherein step (c) further comprises providing the bias power at about 1,800 watts.

EVIDENCE APPENDIX

[NONE]

RELATED PROCEEDINGS APPENDIX

[NONE]